QUADRUPLE RS-485 DIFFERENTIAL LINE DRIVERS

FEATURES

- Designed for TIA/EIA-485, TIA/EIA-422 and ISO 8482 Applications
- Signaling Rates [(1)] up to 30 Mbps
- Propagation Delay Times < 11 ns
- Low Standby Power Consumption 1.5-mA Max
- Output ESD Protection: 12 kV
- Driver Positive- and Negative-Current Limiting
- Power-Up and Power-Down Glitch-Free for Line Insertion Applications
- Thermal Shutdown Protection
- Industry Standard Pin-Out, Compatible With SN75174, MC3487, DS96174, LTC487, and MAX3042

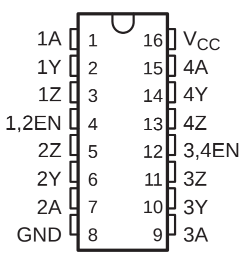
(1) The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

DESCRIPTION

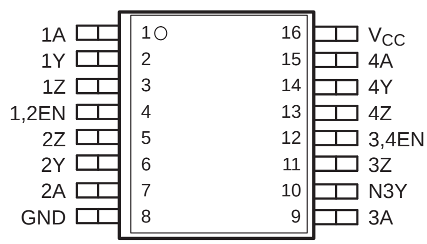
The SN65LBC174A and SN75LBC174A are quadruple differential line drivers with 3-state outputs, designed for TIA/EIA-485 (RS-485), TIA/EIA-422 (RS-422), and ISO 8482 applications.

These devices are optimized for balanced multipoint bus transmission at signaling rates up to 30 million bits per second. The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

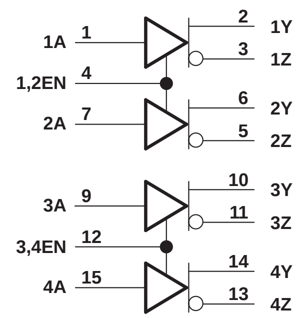
N PACKAGE
(TOP VIEW)



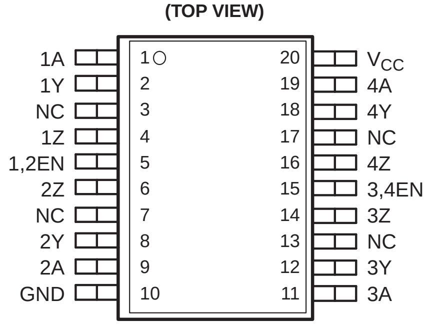
16-DW PACKAGE
(TOP VIEW)



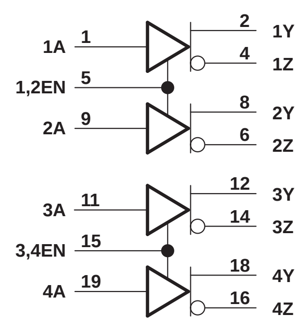
logic diagram (positive logic)



20-DW PACKAGE
(TOP VIEW)



logic diagram (positive logic)



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

Each driver features current limiting and thermal-shutdown circuitry making it suitable for high-speed multipoint applications in noisy environments. These devices are designed using LinBiCMOS®, facilitating low power consumption and robustness.

The two EN inputs provide pair-wise driver enabling, or can be externally tied together to provide enable control of all four drivers with one signal. When disabled or powered off, the driver outputs present a high-impedance to the bus for reduced system loading.

The SN75LBC174A is characterized for operation over the temperature range of 0°C to 70°C. The SN65LBC174A is characterized for operation over the temperature range of -40°C to 85°C.

AVAILABLE OPTIONS

T_A	PACKAGE		
	16-PIN PLASTIC SMALL OUTLINE(1) (JEDEC MS-013)	20-PIN PLASTIC SMALL OUTLINE(1) (JEDEC MS-013)	16-PIN PLASTIC THROUGH-HOLE (JEDEC MS-001)
0°C to 70°C	SN75LBC174A16DW	SN75LBC174ADW	SN75LBC174AN
	MARKED AS 75LBC174A		
40°C to 85°C	SN65LBC174A16DW	SN65LBC174DW	SN65LBC174AN
	MARKED AS 65LBC174A		

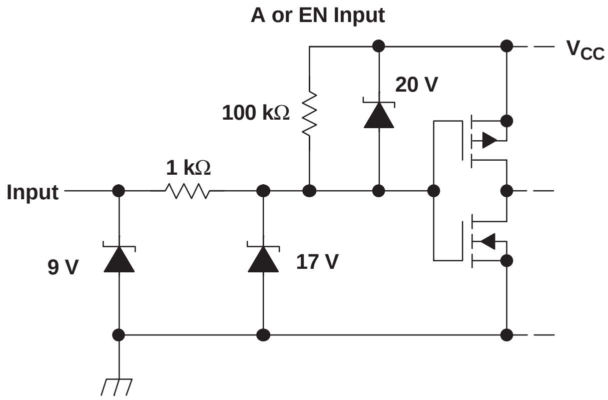
(1) Add R suffix for taped and reeled version.

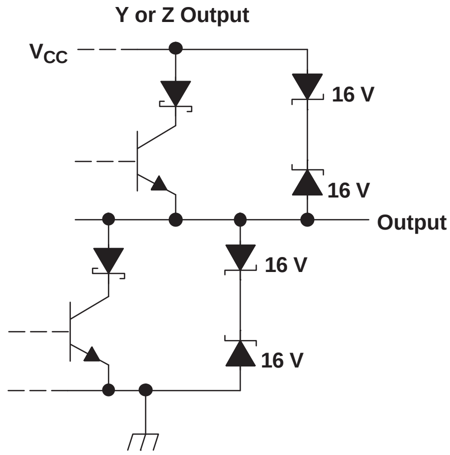
FUNCTION TABLE (EACH DRIVER)(1)

INPUT	ENABLE	OUTPUTS	
A	G	Y	Z
L	H	L	H
H	H	H	L
OPEN	H	H	L
L	OPEN	L	H
H	OPEN	H	L
OPEN	OPEN	H	L
X	L	Z	Z

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off)

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS





ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			UNIT
Supply voltage range, V_{CC} (2)			-0.3 V to 6 V
Voltage range at any bus (DC)			-10 V to 15 V
Voltage range at any bus (transient pulse through 100 Ω, see Figure 8)			-30 V to 30 V
Input voltage range at any A or EN terminal, V_I			-0.5 V to V_{CC} + 0.5 V
Electrostatic discharge	Human body model (3)	Y, Z, and GND	±12 kV
		All pins	±5 kV
	Charged-device model (4)	All pins	±1 kV
Storage temperature range, T_{stg}			-65°C to 150°C
Continuous power dissipation			See Dissipation Rating Table
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			260°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to GND.
(3) Tested in accordance with JEDEC standard 22, Test Method A114-A.
(4) Tested in accordance with JEDEC standard 22, Test Method C101.

DISSIPATION RATING TABLE

PACKAGE(1)	JEDEC BOARD MODEL	$T_A \le 25°C$ POWER RATING	DERATING FACTOR(2) ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
16 DW	LOW K	1200 mW	9.6 mW/°C	769 mW	625 mW
	HIGH K	2240 mW	17.9 mW/°C	1434 mW	1165 mW
20 DW	LOW K	1483 mW	11.86 mW/°C	949 mW	771 mW
	HIGH K	2753 mW	22 mW/°C	1762 mW	1432 mW
16 N	LOW K	1150 mW	9.2 mW/°C	736 mW	598 mW

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal	Y, Z	7		12	V
High-level input voltage, V_{IH}	A, EN	2		V_{CC}	V
Low-level input voltage, V_{IL}	A, EN	0		0.8	V
Output current		60		60	mA
Operating free-air temperature, T_A	SN75LBC174A	0		70	°C
Operating free-air temperature, T_A	SN65LBC174A	40		85	°C

ELECTRICAL CHARACTERISTICS

over recommended operating conditions

PARAMETER		TEST CONDITIONS		MIN	TYP[(1)]	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = -18 mA		-1.5	-0.77		V
V_O	Open-circuit output voltage	Y or Z, No load		0		V_{CC}	V
$\|V_{OD(SS)}\|$	Steady-state differential output voltage magnitude[(2)]	No load (open circuit)		3		V_{CC}	V
		R_L = 54 Ω, See Figure 1		1	1.6	2.5	V
		With common-mode loading, See Figure 2		1	1.6	2.5	V
$\Delta V_{OD(SS)}$	Change in steady-state differential output voltage between logic states	See Figure 1		-0.1		0.1	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 3		2	2.4	2.8	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states	See Figure 3		-0.02		0.02	V
I_I	Input current	A, EN		-50		50	µA
I_{OS}	Short-circuit output current	V_{TEST} = -7 V to 12 V, See Figure 7	V_I = 0 V	-200		200	mA
			V_I = V_{CC}				
I_{OZ}	High-impedance-state output current	V_{TEST} = -7 V to 12 V, See Figure 7	EN at 0 V	-50		50	µA
$I_{O(OFF)}$	Output current with power off	V_{TEST} = -7 V to 12 V, See Figure 7	V_{CC} = 0 V	-10		10	µA
I_{CC}	Supply current	V_I = 0 V or V_{CC}, No load	All drivers enabled			23	mA
			All drivers disabled			1.5	mA

(1) All typical values are at V_{CC} = 5 V and 25°C.
(2) The minimum V_{OD} may not fully comply with TIA/EIA-485-A at operating temperatures below 0°C. System designers should take the possibly lower output signal into account in determining the maximum signal transmission distance.

SWITCHING CHARACTERISTICS

over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	R_L = 54 Ω, C_L = 50 pF, See Figure 4	5.5	8	11	ns
t_{PHL}	Propagation delay time, high-to-low level output		5.5	8	11	ns
t_r	Differential output voltage rise time		3	7.5	11	ns
t_f	Differential output voltage fall time		3	7.5	11	ns
$t_{sk(p)}$	Pulse skew $\|t_{PLH} - t_{PHL}\|$			0.6	2	ns
				0.6	2	
$t_{sk(o)}$	Output skew(1)				2	ns
$t_{sk(pp)}$	Part-to-part skew(2)				3	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	See Figure 5			25	ns
t_{PHZ}	Propagation delay time, high-level-output-to-high impedance				25	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output	See Figure 6			30	ns
t_{PLZ}	Propagation delay time, low-level-output-to-high impedance				20	ns

(1) Output skew ($t_{sk(o)}$) is the magnitude of the time delay difference between the outputs of a single device with all of the inputs connected together.
(2) Part-to-part skew ($t_{sk(pp)}$) is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same input signals, the same supply voltages, at the same temperature, and have identical packages and test circuits.

PARAMETER MEASUREMENT INFORMATION

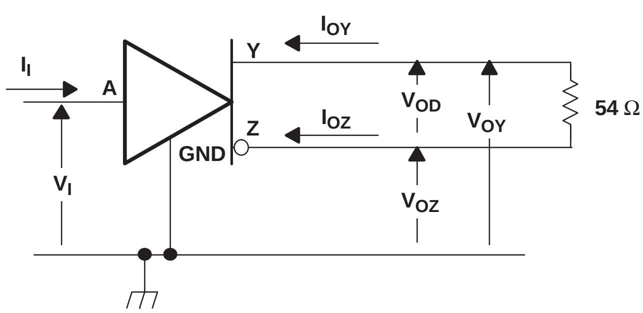


Figure 1. Test Circuit, V_{OD} Without Common-Mode Loading

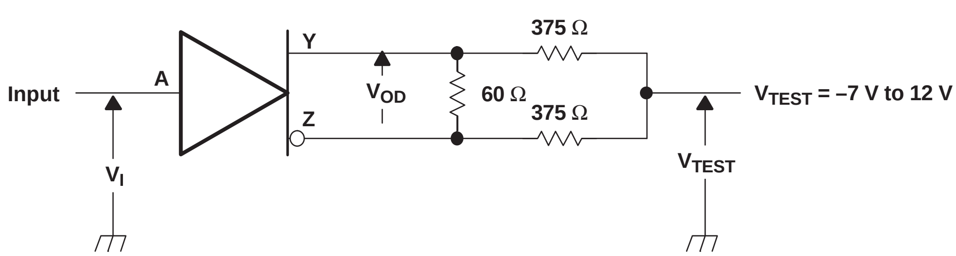
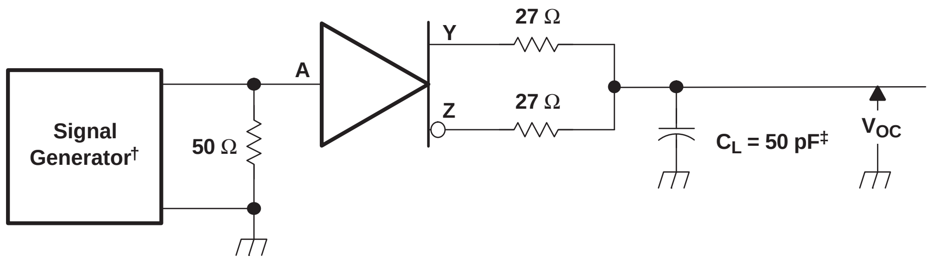


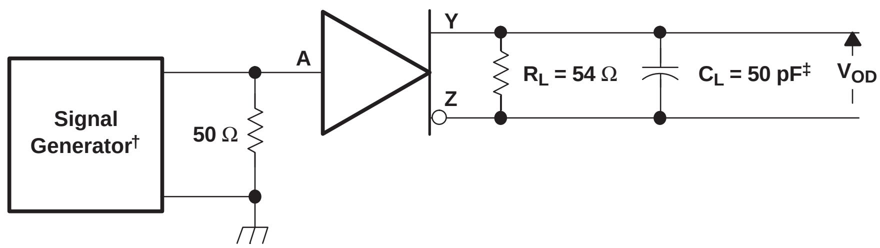
Figure 2. Test Circuit, V_{OD} With Common-Mode Loading

PARAMETER MEASUREMENT INFORMATION (continued)



† PRR = 1 MHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω
‡ Includes probe and jig capacitance

Figure 3. V_{OC} Test Circuit



† PRR = 1 MHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω
‡ Includes probe and jig capacitance

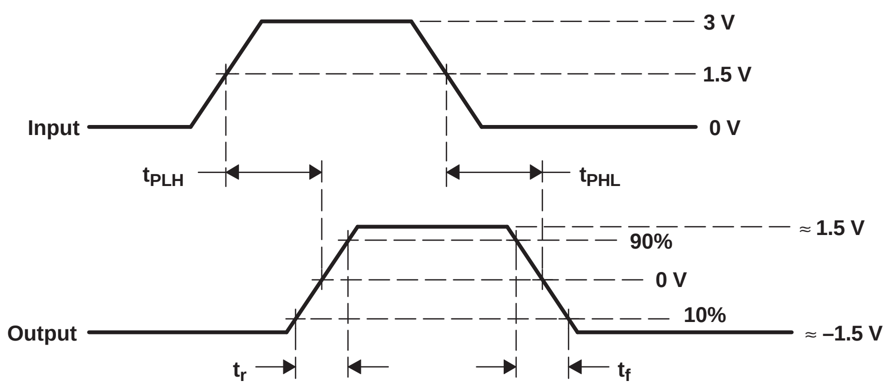
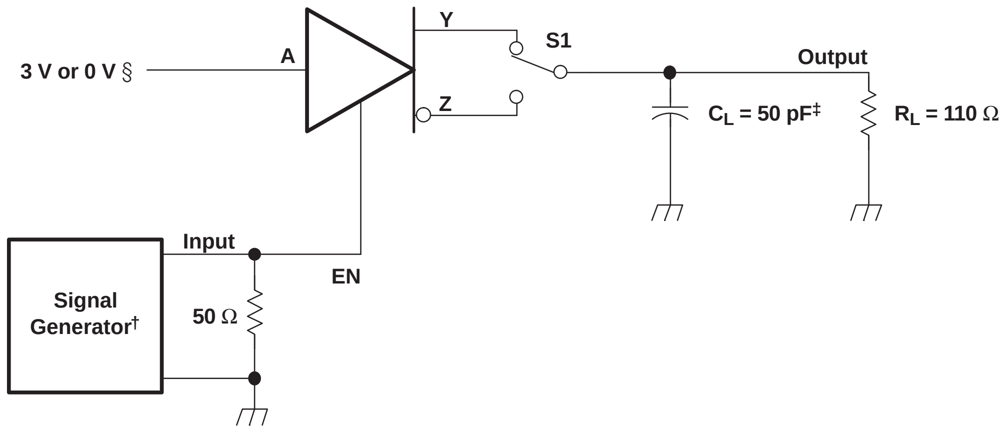


Figure 4. Output Switching Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



† PRR = 1 MHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω
‡ Includes probe and jig capacitance
§ 3 V if testing Y output, 0 V if testing Z output

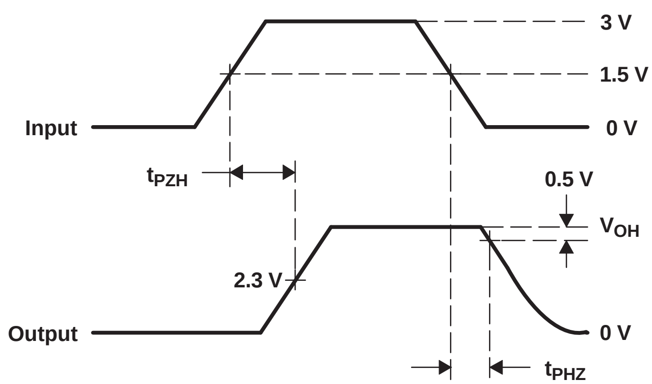
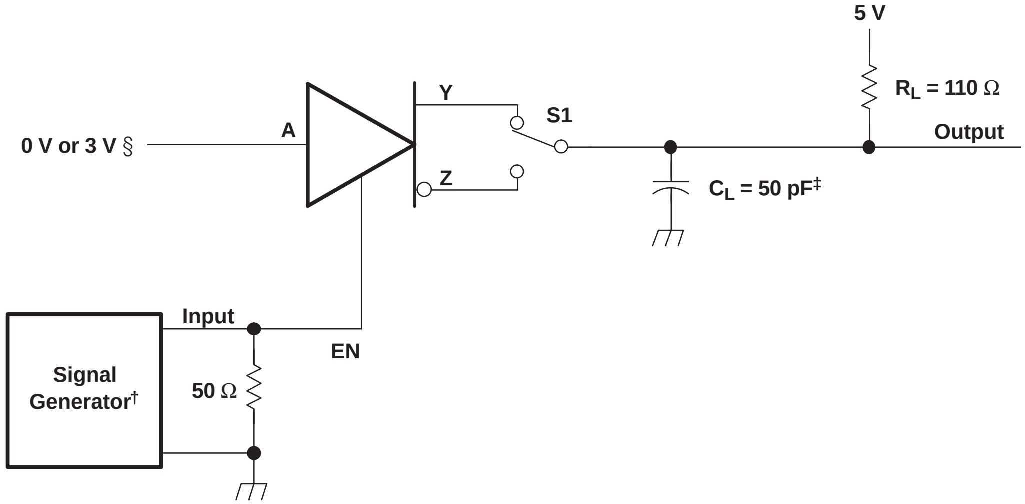


Figure 5. Enable Timing Test Circuit and Waveforms, t_{PZH} and t_{PHZ}

PARAMETER MEASUREMENT INFORMATION (continued)



† PRR = 1 MHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω
‡ Includes probe and jig capacitance
§ 3 V if testing Y output, 0 V if testing Z output

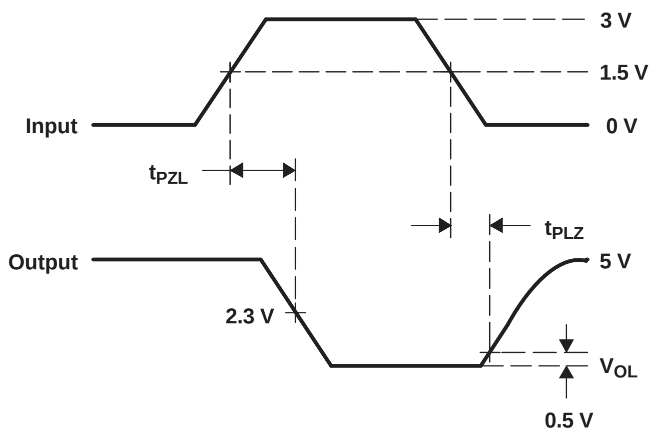


Figure 6. Enable Timing Test Circuit and Waveforms, t_{PZL} and t_{PLZ}

PARAMETER MEASUREMENT INFORMATION (continued)

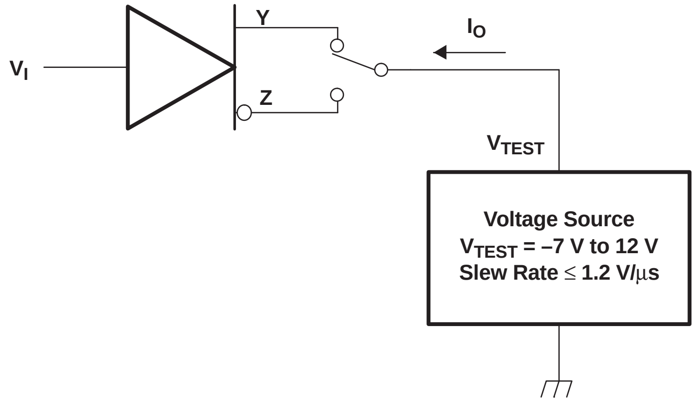


Figure 7. Test Circuit, Short-Circuit Output Current

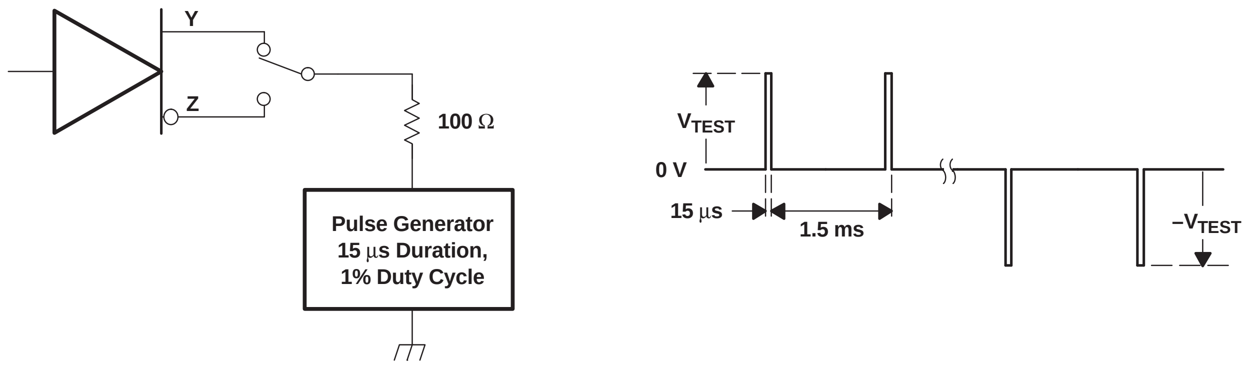


Figure 8. Test Circuit Waveform, Transient Overvoltage Test

TYPICAL CHARACTERISTICS

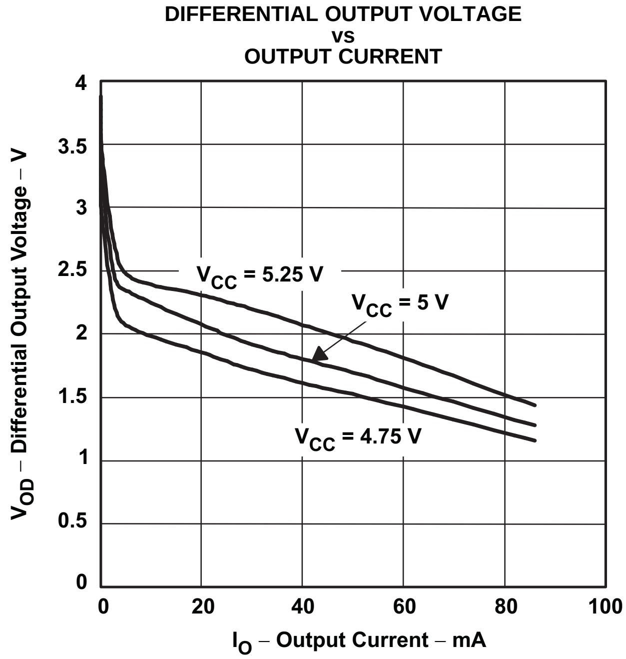


Figure 9.

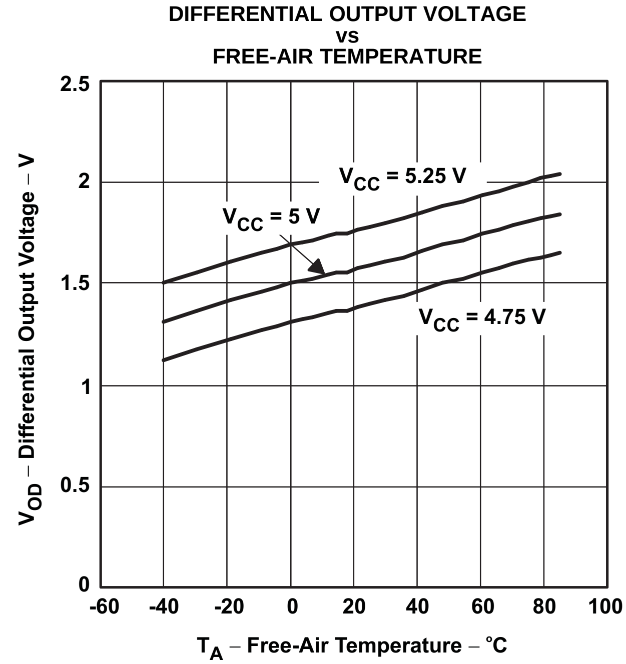


Figure 10.

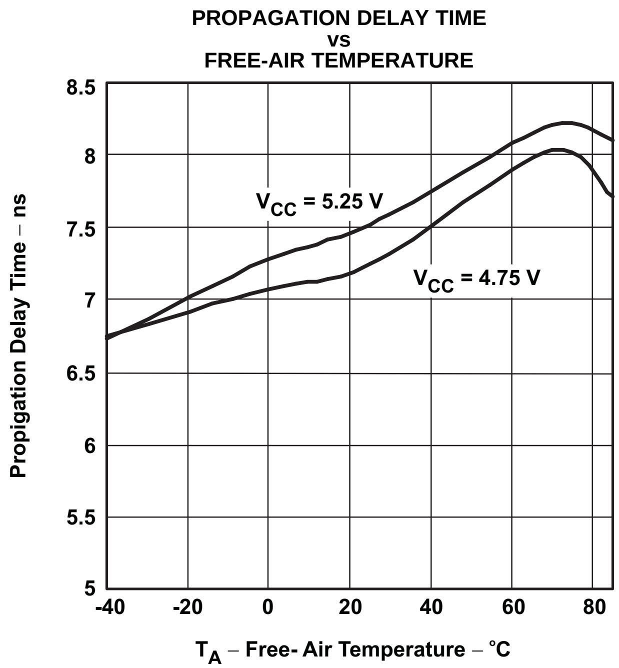


Figure 11.

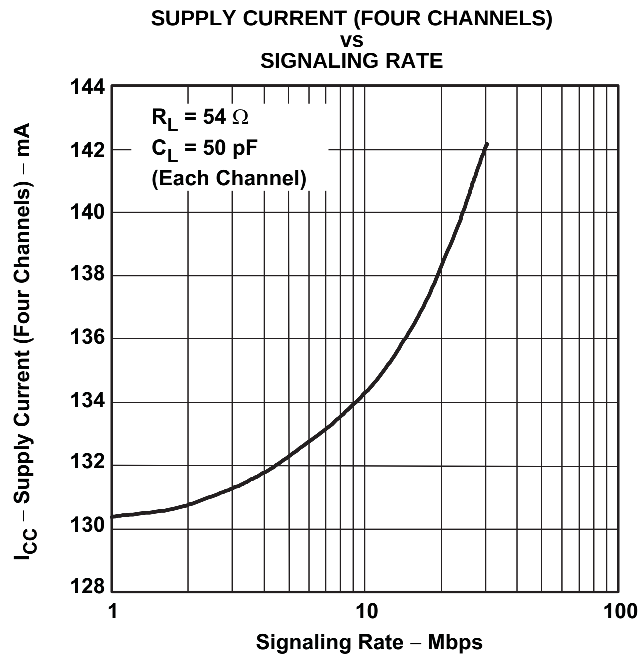


Figure 12.

TYPICAL CHARACTERISTICS (continued)

DIFFERENTIAL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

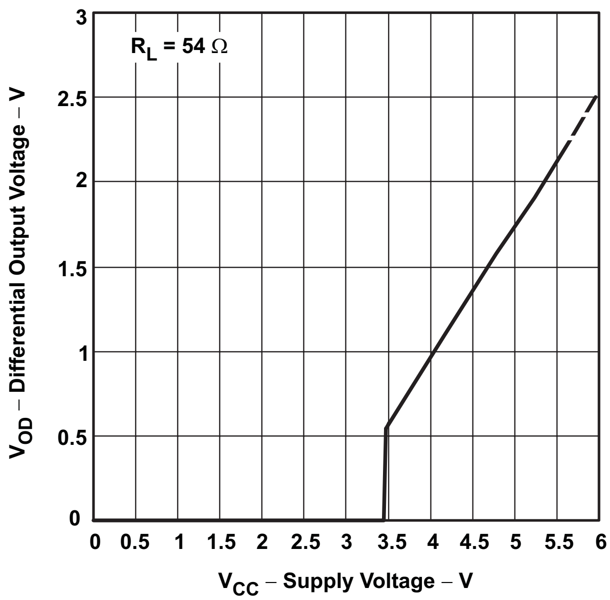


Figure 13.

EYE PATTERN, PSEUDORANDOM DATA AT+ 30 Mbps

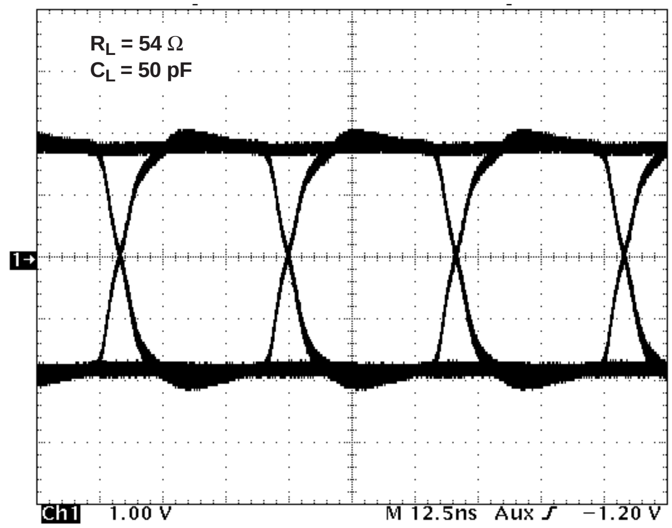


Figure 14.

APPLICATION INFORMATION

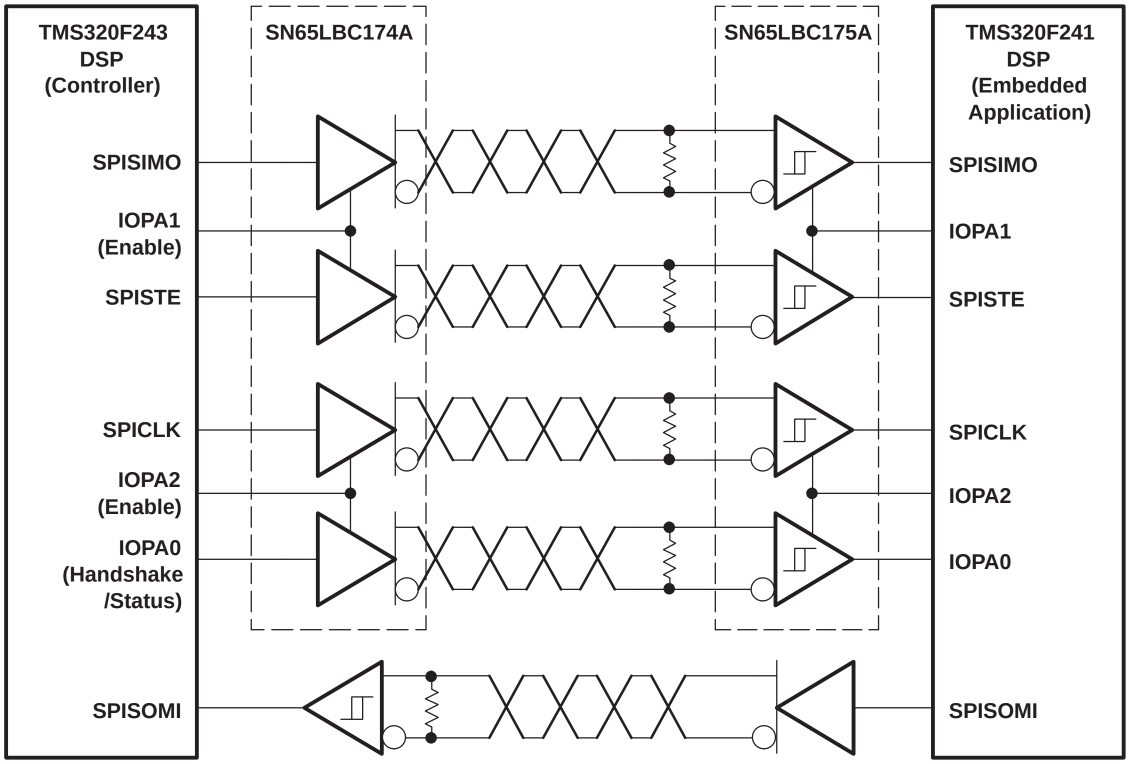


Figure 15. Typical Application Circuit, DSP-to-DSP Link via Serial Peripheral Interface

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN65LBC174A16DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LBC174A16DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LBC174A16DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LBC174A16DWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LBC174ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LBC174ADWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LBC174ADWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LBC174ADWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65LBC174AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPD	N / A for Pkg Type
SN75LBC174A16DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC174A16DWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC174A16DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC174A16DWRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC174ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC174ADWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC174ADWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC174ADWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75LBC174AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPD	N / A for Pkg Type
SN75LBC174ANE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPD	N / A for Pkg Type

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered

at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN65LBC174A :

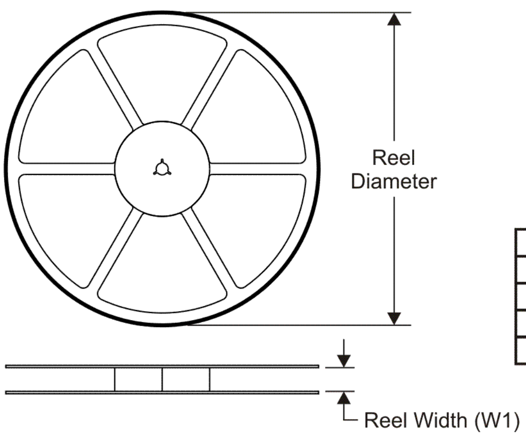
- Enhanced Product: SN65LBC174A-EP

NOTE: Qualified Version Definitions:

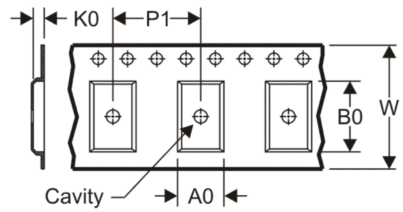
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

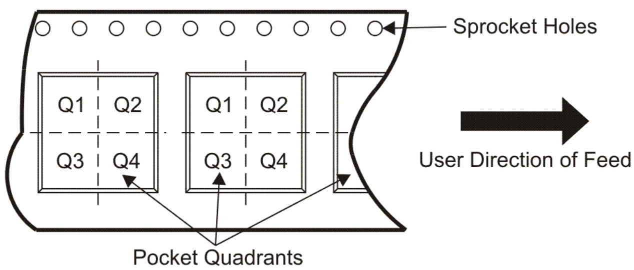


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

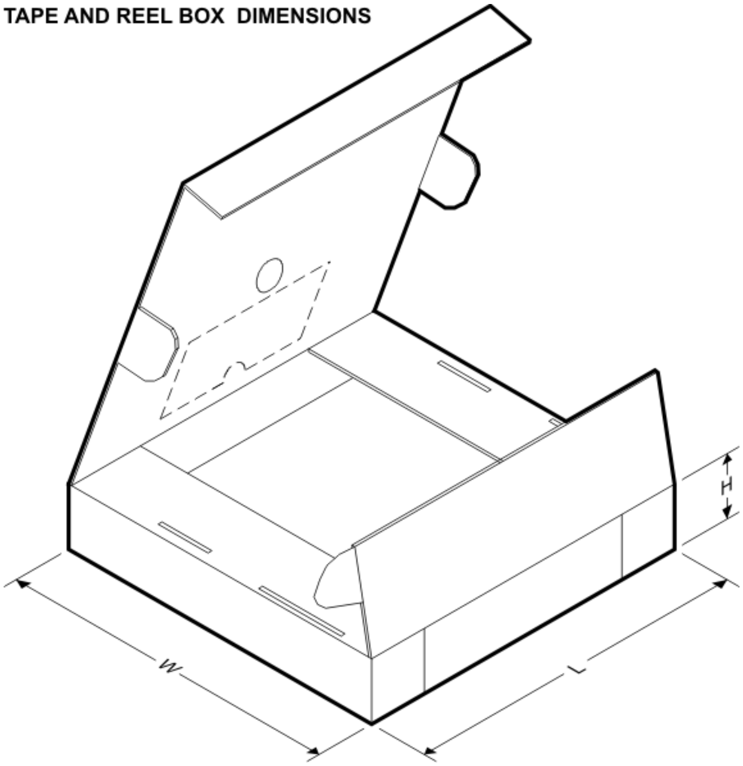
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC174A16DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
SN65LBC174ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.1	2.65	12.0	24.0	Q1
SN75LBC174A16DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
SN75LBC174ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.1	2.65	12.0	24.0	Q1

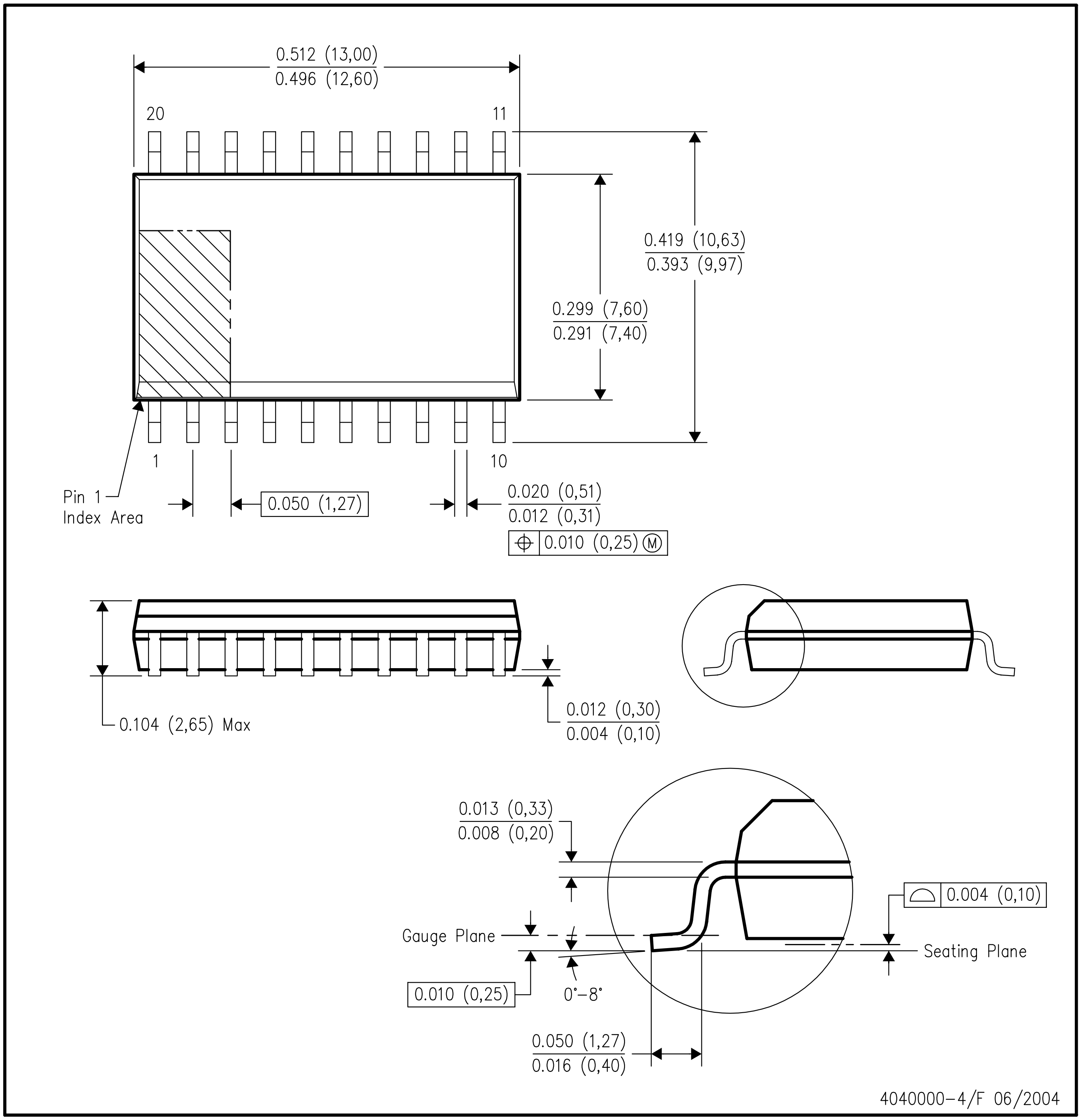
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

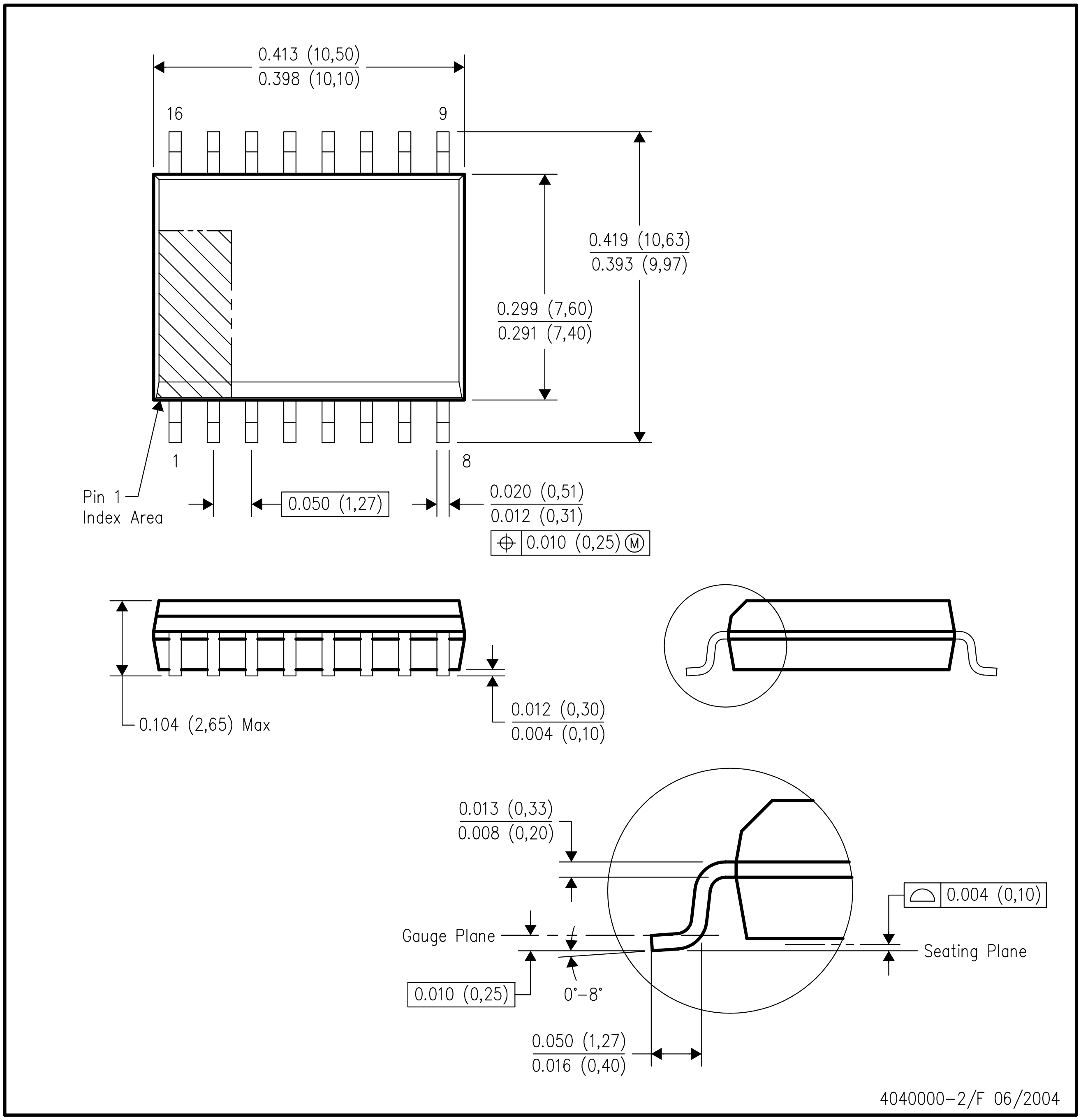
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LBC174A16DWR	SOIC	DW	16	2000	346.0	346.0	33.0
SN65LBC174ADWR	SOIC	DW	20	2000	346.0	346.0	41.0
SN75LBC174A16DWR	SOIC	DW	16	2000	346.0	346.0	33.0
SN75LBC174ADWR	SOIC	DW	20	2000	346.0	346.0	41.0

DW (R-PDSO-G20) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.

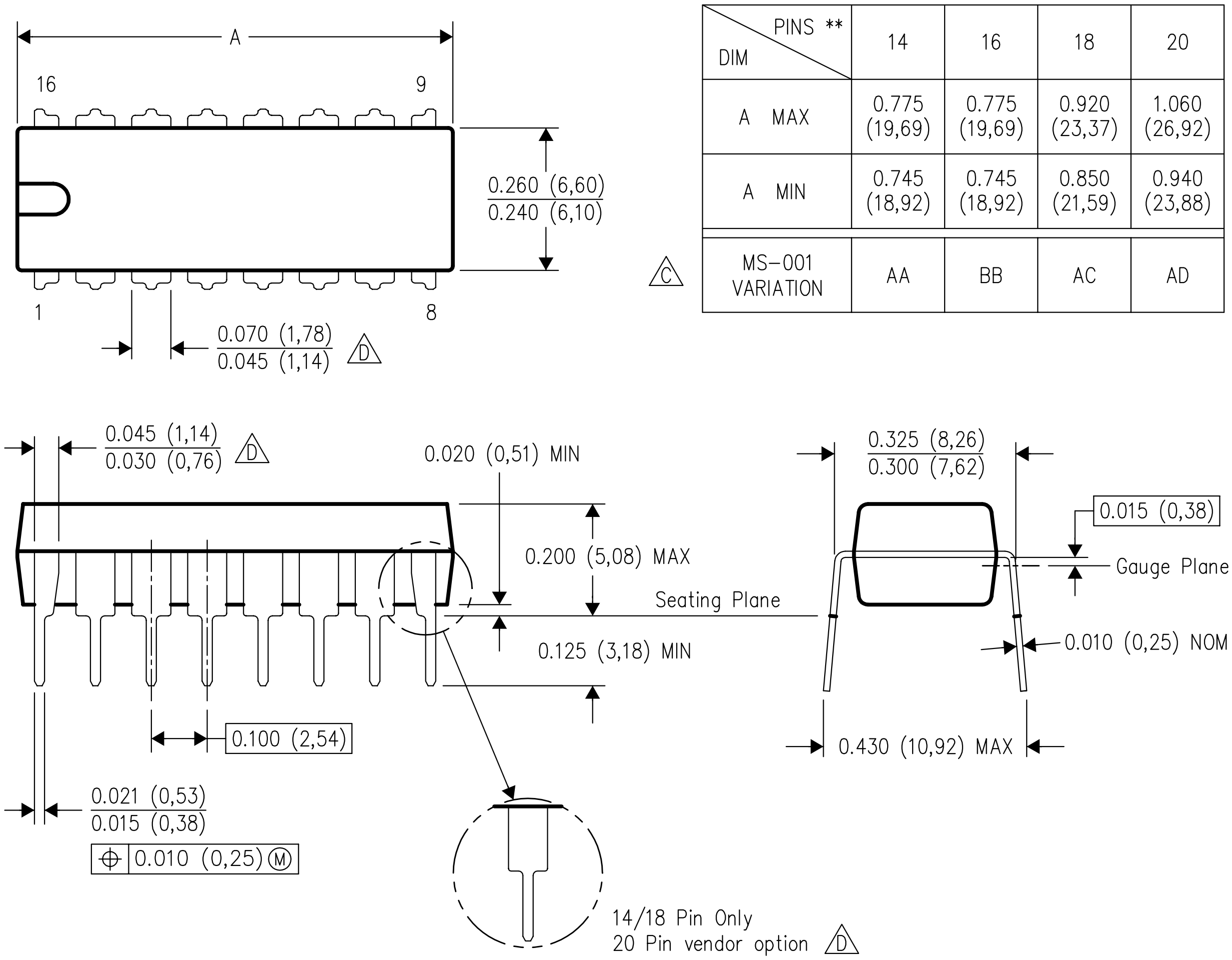
DW (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS–013 variation AA.

N (R-PDIP-T**) PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



PINS ** / DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
(C) MS-001 VARIATION	AA	BB	AC	AD

4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.